TIS-B FPGA Specification Clarification V0.2D

1) **Register extension** according to *TIS-B_InterfaceDesignDocumentV0.4D.doc* 3.1.

2) **Output power**:
   a. Output power has to be configurable in range of 1 to 12 dB in steps of 1 dB.
   b. For this purpose TIS-B Control Register (address 0xE2) bits 3 to 7 are reserved to hold the value.
   c. When output power value has changed, the new value has to be applied for next transmission.

3) **Transmit suppression signal**:
   a. Transmit suppression signal hast to be removed 5 μs ahead of commencing a TIS-B transmission.
   b. Transmit suppression signal has to be enabled immediately after completion of a TIS-B transmission.
   c. Transmit suppression signal should at no time be disabled when receiver protection (4) is disabled.
   d. Transmit suppression signal should be provided on a dedicated pin.

4) **Receiver protection signal**:
   a. Receiver protection signal enable delay is configurable in range of 5 to 100 μs in steps of 1 μs.
   b. Receiver protection signal enable delay value is set in bits 8 to 15 of TIS-B Protection Delay register (address 0xE4).
   c. Receiver protection signal disabled delay is configurable in range of 1 to 100 μs.
   d. Receiver protection signal disable delay value is set in bits 0 to 7 of TIS-B Protection Delay register (address 0xE4).
   e. Change of receiver protection signal delay values will be accepted at the next TIS-B transmission if change happens during a transmission.
   f. TIS-B Control register (address 0xE2) has reserved bit 8 for "keep receiver protection" flag.
   g. If "keep receiver protection" flag is set, receiver protection signal should stay enabled after completion of the TIS-B transmission.
   h. If "keep receiver protection" flag is not set, receiver protection signal should be disabled after the set delay time once TIS-B transmission has completed.
   i. Receiver protection signal should at no time be disabled when transmit suppression signal is disabled.
   j. Receiver protection signal should be provided on a dedicated pin.

5) **Scheduling**:
   a. TIS-B Control register (address 0xE2) has reserved bit 1 for "use time stamp" flag.
   b. Registers 0xDE and 0xE0 are reserved for time stamp value expressed as a value of the 100MHz FPGA counter.
   c. If "use time stamp" bit is set, FPGA has to commence the TIS-B transmission when internal 100MHz counter equals time stamp value of register 0xDE to 0xE0 minus the receiver protection delay value in bit 8 to 15 of the TIS-B Protection Delay register (address 0xE4), if receiver protection is disabled. Otherwise FPGA hast to commence the TIS-B transmission when internal

counter equals time stamp value of register 0xDE to 0xE0 minus 5 µs for transmit suppression signal disabling.

Transmission is discarded and interrupt raised when calculated transmission begin time is smaller than the current counter value and the absolute difference between transmission time and current counter value is less than 20 s.

d. If "use time stamp" bit is not set, FPGA has to commence the TIS-B transmission immediately.

6) **Transmission:**
   a. Register set 0xD0 to 0xE4 will be copied to a shadow register once register 0x71 is written.
   b. All value changes have to be applied for next transmission and have no effect on currently active transmissions.